

**MXD1320 Product Brief**  
**Digital Television Terrestrial Broadcasting**  
**GB20600-2006 Demodulator**  
(Version 1.4)



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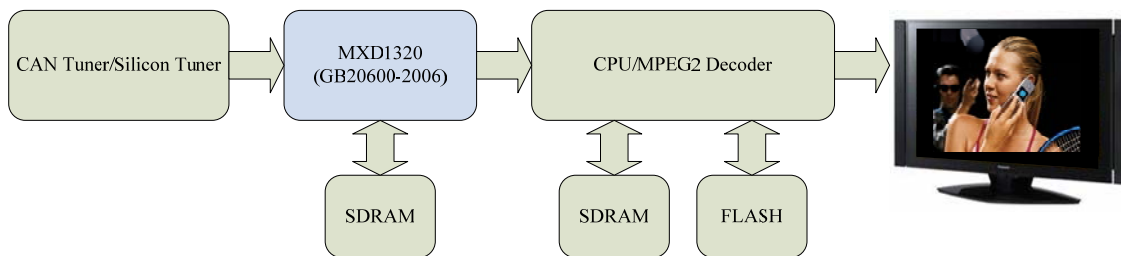
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# 1. Overview

MXD1320 is a demodulator designed for China Digital Television Terrestrial Broadcasting (GB 20600-2006) standard. It is fully compliant with China Digital Television specifications, including both the single-carrier mode and multi-carrier mode. It can totally support 330 modes defined in GB 20600-2006.

The MXD1320 can be integrated into Set-Top Box or DTV set.



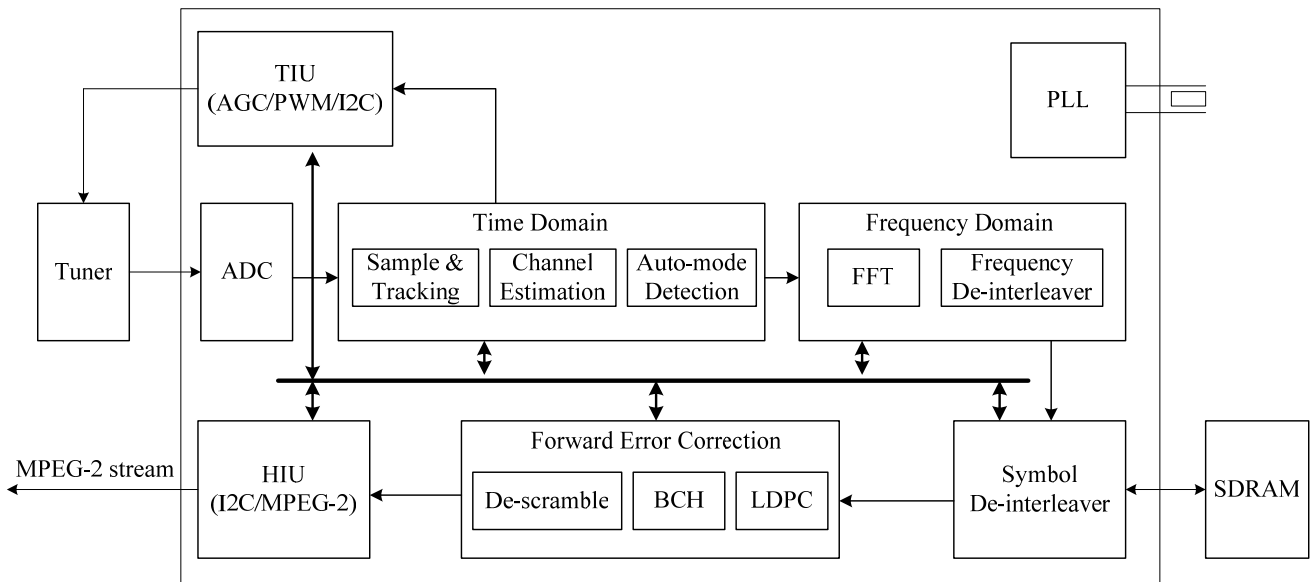
**Figure 1-1 MXD1320 Application System**

## 2. Features

- Fully support China Digital TV Terrestrial Broadcasting System Standard (GB20600-2006)
- Support single and multi carrier receiver solution
- Support dual modes: C = 1, C = 3780
- Modulation modes: 4QAM-NR, 4QAM, 16QAM, 32QAM, 64QAM
- Forward Error Correction Coding Rate: 0.4, 0.6, 0.8
- Symbol de-interleave : none, 240, 720
- Guard Interval: 420 (fixed/rotate phase), 595, 945 (fixed/rotate phase)
- Automatic transmission mode detection and synchronization
- Integrated low power dual-channel 10-bit ADC
- Support 16.384/24.576MHz oscillator
- Support of ZIF, LIF (8.192MHz) and IF (36MHz) input from tuner
- I2C master and PWM AGC for tuner control
- Flexible host interfaces including MPEG2-TS serial/parallel and I2C
- High performance: -97dbm sensitivity
- Fast TPS acquisition: < 100ms
- Ultra compact package: 128pin LQFP(14x14x1.4mm3)(MXD1320)
- Low power consumption: < 150mW (including ADC)
- Excellent ability to resist multi-path interference and Doppler effect

### 3. Block Diagram

The MXD1320 top level functional block diagram is shown in Figure 3-1.



**Figure 3-1 Functional Block Diagram**

The demodulator consists of embedded ADC and PLL, time domain module, frequency domain module, symbol de-interleave module, forward error correction module, tuner and host interface unit.

The demodulator use AGC and PWM method to control the tuner, get the baseband I Q signal. The embed ADC translate the analog I Q signal to digital signal. There are three submodule in the time domain. If there is one channel in the air, Time domain module response for sample and tracking, do some channel estimation job, auto detect the channel mode and channel parameter, such as fine frequency offset , sampling frequency offset and frame identify(FID).

After time domain there is the frequency domain module, which is responsible for some FFT and frequency de-interleave jobs and get some digital data. Then these digital data be sent to Symbol De-Interleave module, it do some symbol de-interleave job by using of SDRAM.

The FEC decoder consists of LDPC, BCH decoder and De-scramble decoder.

The HIU (Host Interface Unit) supports I<sup>2</sup>C, and MPEG2 TS serial and parallel interfaces.

## 4. Pins & Package

### 4.1. Pin Assignment

MP2TS_D5	97	64	SDR_D15
MP2TS_D4	98	63	SDR_D14
VDDIO_H	99	62	VDDIO_SDR
MP2TS_D3	100	61	SDR_D13
VSS	101	60	SDR_D12
MP2TS_D2	102	59	SDR_D11
MP2TS_D1	103	58	SDR_D10
VDD	104	57	VSS
MP2TS_D0	105	56	SDR_D9
MP2TS_SYNC	106	55	SDR_D8
MP2TS_VLD	107	54	SDR_WE
VDDIO_H	108	53	SDR_CAS
MP2TS_CLK	109	52	SDR_RAS
VSS	110	51	SDR_ADD1
SYS_RST	111	50	SDR_ADD3
VSS	112	49	SDR_ADD5
N/C	113	48	SDR_ADD7
VSS	114	47	SDR_ADD9
VDD	115	46	VDD
N/C	116	45	VSS
N/C	117	44	VDDIO_SDR
VDDIO_H	118	43	VDD
N/C	119	42	SDR_D7
N/C	120	41	SDR_D6
VDD	121	40	VSS
N/C	122	39	SDR_D5
PLI_LD	123	38	SDR_D4
VSS	124	37	SDR_D3
JTAG_TDO	125	36	SDR_D2
JTAG_TDI	126	35	SDR_D1
JTAG_TMS	127	34	SDR_D0
JTAG_TCK	128	33	VDDIO_SDR
AVDDPH	1		
VINPI	2		
AGND	3		
VINPQ	4		
VINNQ	5		
AGND	6		
AVDDI	7		
VCM	8		
VREFP	9		
VREFN	10		
VRG	11		
N/C	12		
N/C	13		
VDD	14		
VSS	15		
TIU_CLK	16		
TIU_DATA	17		
N/C	18		
VDD	19		
N/C	20		
AGC_CTRU	21		
VSS	22		
OSC_XI	23		
OSC_XO	24		
VDDIO_T	25		
VDDIO_P	26		
AVDDP	27		
AVSSP	28		
AVDDP	29		
AVSSP	30		
VDDP	31		
VSSP	32		
MP2TS_D6	96		
MP2TS_D7	95		
VSS	94		
N/C	93		
HIU_SDA	92		
HIU_SCL	91		
HIU_I2C_ADDR	90		
PLI_PD	89		
TM2	88		
TM1	87		
TM0	86		
CRYS_SFI	85		
VDD	84		
SDR_DM0	83		
SDR_BA1	82		
SDR_BA0	81		
VSS	80		
VDDIO_SDR	79		
SDR_ADD2	78		
SDR_ADD4	77		
SDR_ADD6	76		
SDR_ADD8	75		
VDD	74		
SDR_ADD10	73		
VSS	72		
SDR_CLK	71		
VDDIO_SDR	70		
SDR_CS	69		
SDR_ADD0	68		
SDR_ADD11	67		
SDR_CKE	66		
SDR_DM1	65		

**MXD1320 GB20600-2006**  
**Demodulator**

Figure 4-1 MXD1320 128 Pin LQFP Package

## 4.2. Pin Description

### Note

Type:

*DI* (digital input), *DO* (digital output), *DIO* (digital bidirectional), *DP* (digital power), *DG* (digital ground), *AI* (analog input), *AO* (analog output), *AIO* (analog bidirectional), *AP* (analog power), *AG* (analog ground), *PD* (pull down), *PU*<sup>1</sup> (pull up), *S* (Schmitt trigger input)

### 4.2.1. Power Supply

PIN_NAME	PIN_NUM	Type	Description
Common power supply			
VSS	15,22,40,45,57,72,80,94,101,110,124	DG	Digital ground
VDD	14,43,46,74,84,104,115, 121	DP	Core digital power supply(1.2V)
HIU IO power supply			
VDDIO_H	108,118	DP	HIU IO power supply(3.3V)
TIU IO power supply			
VDDIO_T	25	DP	TIU IO power supply(3.3V)
SDRAM interface IO power			
VDDIO_SDR	33,44,62,70,79	DP	SDRAM interface power supply(3.3V)
PLL power			
VDDIO_P	26	DP	PLL interface IO power(3.3V)
AVDD_P	27,29	AP	Internal PLL analog power(1.2V)
VDD_P	31	DP	Digital power(1.2V)
VSS_P	32	DG	Digital ground
AVSS_P	28,30	AG	Internal PLL analog ground
Analog 3.3V Power supply			
AGND	4	AG	Analog 3.3V power domain ground
AVDDH	1	AP	Analog 3.3V power domain power
Analog 1.2V Power supply			
AGND	7	AG	Analog 1.2V power domain ground
AVDDL	8	AP	Analog 1.2V power domain power

## 4.2.2.I2C interface

PIN_NAME	PIN_NUM	Type	Description
Host I2C serial bus			
HIU_I2C_ADD	90	DI	HIU I <sup>2</sup> C address LSB
HIU_SCL	91	DI,S,PU	I <sup>2</sup> C serial clock
HIU_SDA	92	DIO,S,PU	I <sup>2</sup> C serial data
Tuner I2C serial bus			
TIU_CLK	16	DIO,PU	I <sup>2</sup> C serial clock to tuner
TIU_DATA	17	DIO,PU	I <sup>2</sup> C serial data to tuner

## 4.2.3.AGC control interface

PIN_NAME	PIN_NUM	Type	Description
AGC controller			
AGC_CTRL	21	DO	AGC control signal

## 4.2.4.TS interface

PIN_NAME	PIN_NUM	Type	Description
MPEG2 TS			
MP2TS_CLK	109	DO	MPEG2 TS Clock
MP2TS_DATA7-0	95,96,97,98,100,102,103	DO	MPEG2 TS Data
MP2TS_SYNC	106	DO	MPEG2 TS Sync signal
MP2TS_VLD	107	DO	MPEG2 TS Valid signal

## 4.2.5.SDRAM interface

PIN_NAME	PIN_NUM	Type	Description
Host SDRAM bus			
SDR_ADD11-0	67,73,47,75,48,76,49,77, 50,78, 51, 68,	DO	Extern SDRAM address selection
SDR_D15-0	64,63,61,60,59,58,56,55,4 2,41,39,38,37,36,35,34	DIO	Extern SDRAM memory data
SDR_CLK	71	DO	Extern SDRAM memory clock
SDR_CS	69	DO	Extern SDRAM chip select
SDR_BA0-1	81,82	DO	Extern SDRAM bank select
SDR_CKE	66	DO	Extern SDRAM CKE signal
SDR_DQM1-0	65,83	DO	Extern SDRAM DQM signal

SDR_WE	54	DO	Extern SDRAM WE signal
SDR_CAS	53	DO	Extern SDRAM CAS signal
SDR_RAS	52	DO	Extern SDRAM RAS signal

#### 4.2.6. Analog signal interface

PIN_NAME	PIN_NUM	Type	Description
Analog reference voltage			
VBG	12	AIO	Connect to bandgap decoupling capacitor VBG: BandGap Voltage
VREFP	10	AIO	ADC positive reference voltage
VREFN	11	AIO	ADC negative reference voltage
VCM	9	AIO	ADC common voltage
Analog signal input			
VINPI	3	AI	Positive input of I-ADC
VINNI	2	AI	Negative input of I-ADC
VINPQ	5	AI	Positive input of Q-ADC
VINNQ	6	AI	Negative input of Q-ADC

#### 4.2.7. System mode select

PIN_NAME	PIN_NUM	Type	Description
System reset			
SYS_RST	111	DI,S,PU	Reset, active low
System mode select			
CRYS_SEL	85	DI	Extern crystal select
TM0	86	DI,PD	Connect to ground
TM1	87	DI,PD	Connect to ground
TM2	88	DI,PD	Connect to ground

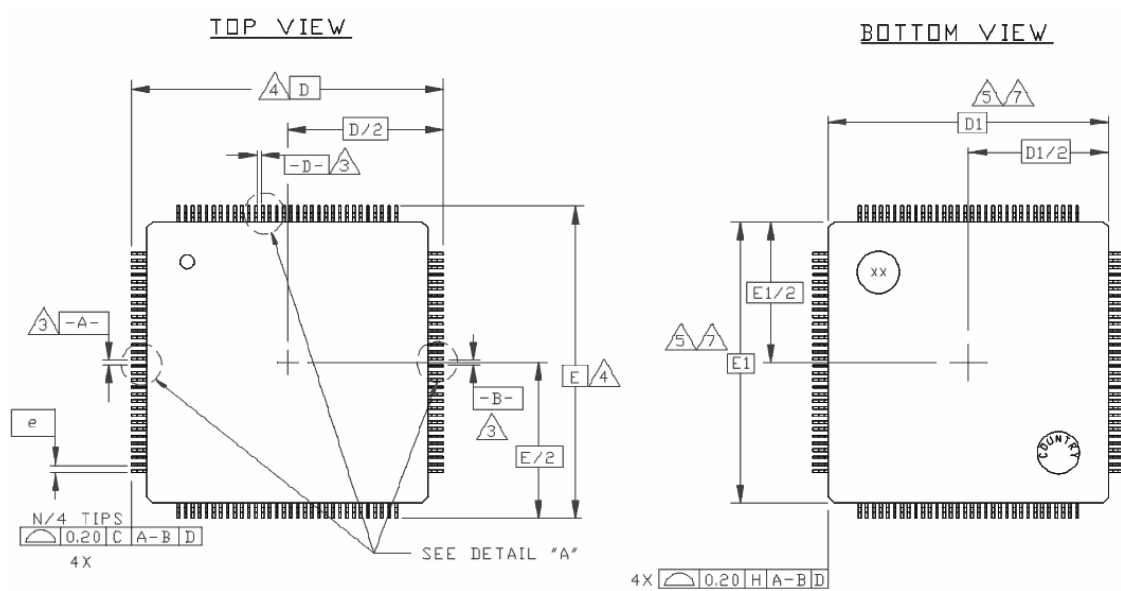
#### 4.2.8. PLL Signal

PIN_NAME	PIN_NUM	Type	Description
PLL			
PLL_LD	123	DO	PLL lock detection, high means PLL is locked
PLL_PD	89	DI	PLL power down, high means power down

<sup>1</sup> Both pull up and pull down(PU/PD) have weak pull strength. The resistor is about 30 KOhm. External resistor may be used if stronger pull strength is required.

### 4.3. Package Dimension

Note: Unit in mm.



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE	
	MIN.	NOM.	MAX.		
	A	~	~		1.60
A <sub>1</sub>	0.05	~	0.15		
A <sub>2</sub>	1.35	1.40	1.45		
D	16.00 BSC.				
D <sub>1</sub>	14.00 BSC.				
E	16.00 BSC.				
E <sub>1</sub>	14.00 BSC.				
L	0.45	0.60	0.75		
N	*128				
e	0.40 BSC.				
b	0.13	0.18	0.23	9	
b <sub>1</sub>	0.13	0.16	0.19		
ccc	~	~	0.08		
ddd	~	~	0.07		

Figure 4-2 Chip Top and Bottom View