

MXD0120 Product Brief
DAB/DAB+/T-DMB demodulator
(Version 1.2)



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1. Overview

The MXD0120 is a mobile digital TV demodulator chip designed for the DAB, DAB+, DAB-IP and T-DMB applications.

The MXD0120 accepts IF/low IF or zero IF signal from the RF tuner device. The decoded MSC and FIC data are sent out through high speed serial interface such as SPI, SDIO or MPEG2 TS.

The MXD0120 consists of low-power dual-channel 10-bit ADC, OFDM demodulator, full capacity time de-interleaver, Viterbi decoder, Reed-Solomon decoder, outer de-interleaver, and time/frequency synchronization unit. By integrating the ADC and outer decoder (Reed-Solomon decoder and the outer de-interleaver), the MXD0120 fully supports the T-DMB/DAB+ application with minimum load on the host processor.

The MXD0120 is also suited for the DAB-IP application with the support of the packet data mode.

The MXD0120 provides serial interface through which the companion RF tuner can be configured by the host. The tuner interface of the MXD0120 is designed to have enough flexibility to support most existing RF tuner devices.

The MXD0120 supports all the popular serial interfaces used in the mobile multimedia applications including SPI, SDIO and MPEG2 TS. An I²C interface is also provided for exchanging control and status information with the host.

The MXD0120 employs advanced low power design techniques and implements power cycling control of the ADC and tuner to reduce the system power consumption to the minimum. A full hardwired ASIC design assures MXD0120 the smallest size and the highest power efficiency.

The MXD0120 can be used in DAB/DAB+/T-DMB/DAB-IP receivers including portable multimedia player, PDA, mobile phone, automobile entertainment system, PC add-on cards, USB dongle, and digital camera. It is best suited for mobile application with low power consumption and small foot-print requirements.

2. Features

- Fully compliant with ETSI EN 300 401 (DAB), ETSI TS 102 427/428 (DMB), GY/T 214-2006 and ETSI TS 102 563 (DAB+).
- Support of all DAB transmission modes (I, II, III, and IV)
- Automatic mode detection and frame synchronization.
- Integrated low power dual-channel 10-bit ADC.
- Integrated outer decoder, including the outer de-interleaver and Reed-Solomon decoder, required for T-DMB and DAB+ service.
- Support of dynamic multiplex re-configuration.
- TII (Transmitter Identification Information) decoding capability.
- Robust reception with effective frequency/timing synchronization and offset compensation algorithm.
- Dual-channel simultaneous demodulation with each channel carries any of the audio, video and packet data.
- Fast channel acquisition (< 200 ms).
- Embedded SRAM supporting full channel capacity decoding corresponding to 1.8 Mbps data rate.
- Buffered outputs reducing the transaction frequency and host load.
- Support of zero-IF (I/Q), low IF (1.024/2.048 MHz) and IF (38.912 MHz) input from tuner.
- Support up to ± 192 KHz frequency offset correction.
- I2C master, PWM AGC and power cycling signals for tuner control.
- Flexible host interfaces including SPI, SDIO, MPEG2 TS serial and I2C.
- 24.576 MHz input clock.
- 1.2V (core) and 1.8-3.3V (I/O) supply voltages.
- Extremely compact 5x5 mm² BGA package with 65 balls.
- Low power consumption, (Only 18mW when full capacity reception)

3. Block Diagram

The MXD0120 top level functional block diagram is shown in Figure 3-1.

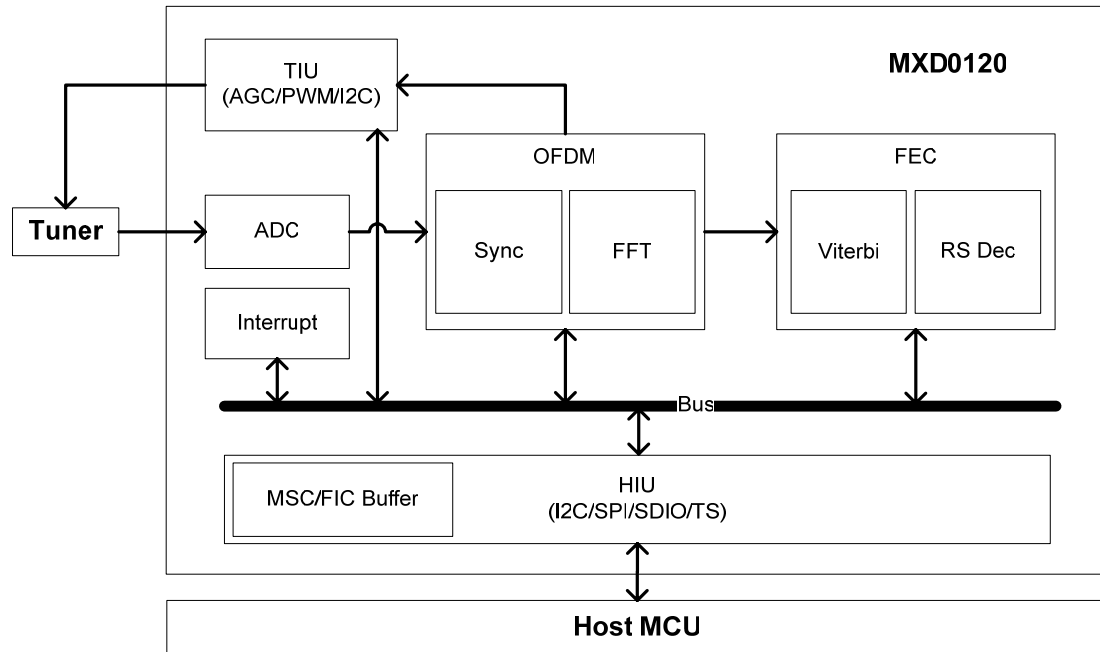


Figure 3-1 Functional Block Diagram

The OFDM demodulator consists of synchronization module, FFT and DQPSK de-mapper. The FEC decoder consists of de-interleaver, Viterbi decoder and RS (Reed-Solomon) decoder. The TIU (Tuner Interface Unit) consists of AGC/PWM control logic and tuner access control unit. The HIU (Host Interface Unit) supports I²C, SPI, SDIO and MPEG2 TS serial interface.

4. Pins & Package

4.1. Pin Assignment

TOP VIEW

A1 REV8	A2 REV6	A3 REV4	A4 TS _DATA	A5 TS_VLD	A6 REV2	A7 REV0	A8 VDDIO _H	A9 HIU_I2C_ ADDR
B1 REV9	B2 REV7	B3 REV5	B4 TS_CLK	B5 TS _SYNC	B6 REV3	B7 VDD	B8 REV1	B9 VSS
C1 REV11	C2 REV10						C8 HIU _SCL	C9 HIU _SDA
D1 MOD1	D2 SYS _CLK		D4 VSS	D5 VDDIO _H	D6 VSS		D8 RSTN	D9 SDIO _DATA3
E1 VSS	E2 MOD0		E4 VDD	E5 VSS	E6 VDD		E8 SDIO _DATA2	E9 SDIO _DATA1
F1 VDDIO _T	F2 AGC _CTRL		F4 TUNER _LPC	F5 TIU _DATA	F6 AGND		F8 SDIO _DATA0	F9 SDIO _CMD
G1 VSS	G2 AGC _HOLD						G8 SDIO _CLK	G9 VDD
H1 TIU _CLK	H2 VININ	H3 VINQP	H4 AGND	H5 AVDDL	H6 VREFP	H7 VBG	H8 VSS	H9 VDDIO _H
J1 AVDDH	J2 VINIP	J3 VINQN	J4 VCM	J5 VREFN	J6 REVA	J7 VDD	J8 VDDIO _H	J9 VSS

Figure 4-1 MXD0120 65 Pin BGA Package

4.2. Pin Description

Note

Type:

DI (digital input), *DO* (digital output), *DIO* (digital bidirectional), *DP* (digital power), *DG* (digital ground), *AI* (analog input), *AO* (analog output), *AIO* (analog bidirectional), *AP* (analog power), *AG* (analog ground), *PD* (pull down), *PU*¹ (pull up), *S* (Schmitt trigger input)

PIN_NAME	PIN_NUM	Type	Description
Common power supply			
VSS	D4,B9,D6, E1,E5,G1, H8,J9	DG	Digital ground
VDD	B7,E4,E6, G9,J7	DP	Core digital power supply(1.2V)
HIU IO power supply			
VDDIO_H	A8,D5, H9,J8	DP	HIU IO power supply
System signal in HIU IO power domain			
RSTN	D8	DI,S,PU	Reset, active low
Host I2C serial bus			
HIU_I2C_ADDR	A9	DI	HIU I ² C address LSB
HIU_SCL	C8	DI,S,PU	I ² C serial clock
HIU_SDA	C9	DIO,S, PU	I ² C serial data
HIU SDIO/SPI			
SDIO_CLK	G8	DI	SDIO clock or SPI clock
SDIO_CMD	F9	DIO,PU	SDIO command signal or SPI MOSI
SDIO_DATA0	F8	DO,PU	SDIO data[0] or SPI MISO
SDIO_DATA1	E9	DO,PU	SDIO data[1] or Interrupt
SDIO_DATA2	E8	DIO,PU	SDIO data[2] or SPI mode select
SDIO_DATA3	D9	DIO	SDIO data[3] or SPI CS

Table 4-1 Pin Description (Part I)

PIN_NAME	PIN_NUM	Type	Description
HIU TS			
TS_CLK	B4	DO	MPEG2 TS Clock
TS_DATA	A4	DO	MPEG2 TS Data
TS_SYNC	B5	DO	MPEG2 TS Sync signal
TS_VLD	A5	DO	MPEG2 TS Valid signal
RESERVED Pin			
REV11~0	C1, C2,B1, A1, B2,A2, B3, A3,B6, A6, B8, A7	DI	Connect to ground.
TIU IO Power supply			
VDDIO_T	F1	DP	TIU IO power supply
System signal in TIU IO power domain			
SYS_CLK	D2	DI	System clock
MOD0	E2	DI,PD	Connect to ground
MOD1	D1	DI,PD	Connect to ground
TIC_CLK	H1	DIO,PU	I ² C serial clock
TIC_DATA	F5	DIO,PU	I ² C serial data
AGC controller			
AGC_CTRL	F2	DO	AGC control signal
AGC_HOLD	G2	DO	AGC hold signal
TUNER_LPC	F4	DO	Tuner Low Power Control
Analog 3.3V Power supply			
AGND	H4	AG	Analog 3.3V power domain ground
AVDDH	J1	AP	Analog 3.3V power domain power
Analog signal			
VINIP	J2	AI	Positive input of I-ADC
VININ	H2	AI	Negative input of I-ADC
VINQP	H3	AI	Positive input of Q-ADC
VINQN	J3	AI	Negative input of Q-ADC
Analog 1.2V Power supply			
AGND	F6	AG	Analog 1.2V power domain ground
AVDDL	H5	AP	Analog 1.2V power domain power

Table 4-2 Pin Description (Part II)

PIN_NAME	PIN_NUM	Type	Description
Analog signal			
VBG	H7	AIO	Connect to bandgap decoupling capacitor VBG: BandGap Voltage
VREFP	H6	AIO	ADC positive reference voltage
VREFN	J5	AIO	ADC negative reference voltage
VCM	J4	AIO	ADC common voltage
REVA	J6	AIO	Reserved. Don't connect.

Table 4-3 Pin Description (Part III)

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- 1 Both pull up and pull down(PU/PD) have weak pull strength. The resistor is about 30 KOhm. External resistor may be used if stronger pull strength is required.
 - 2 SDIO and SPI ports share the same IO pins. The chip works in either SDIO mode or SPI mode.

4.3. Package Dimension

Note: Unit in mm.

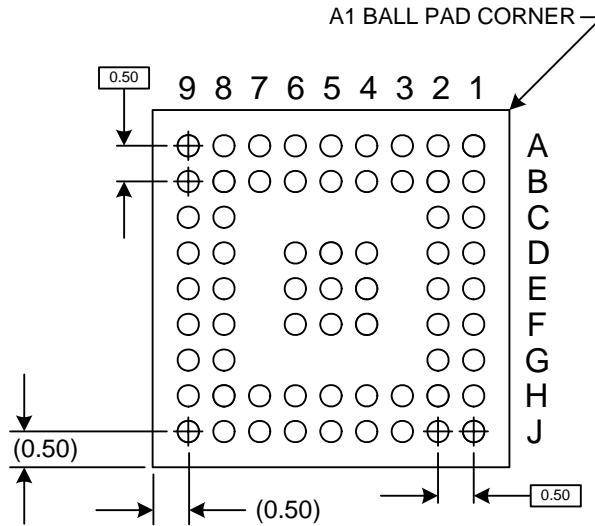


Figure 4-2 Chip Bottom View

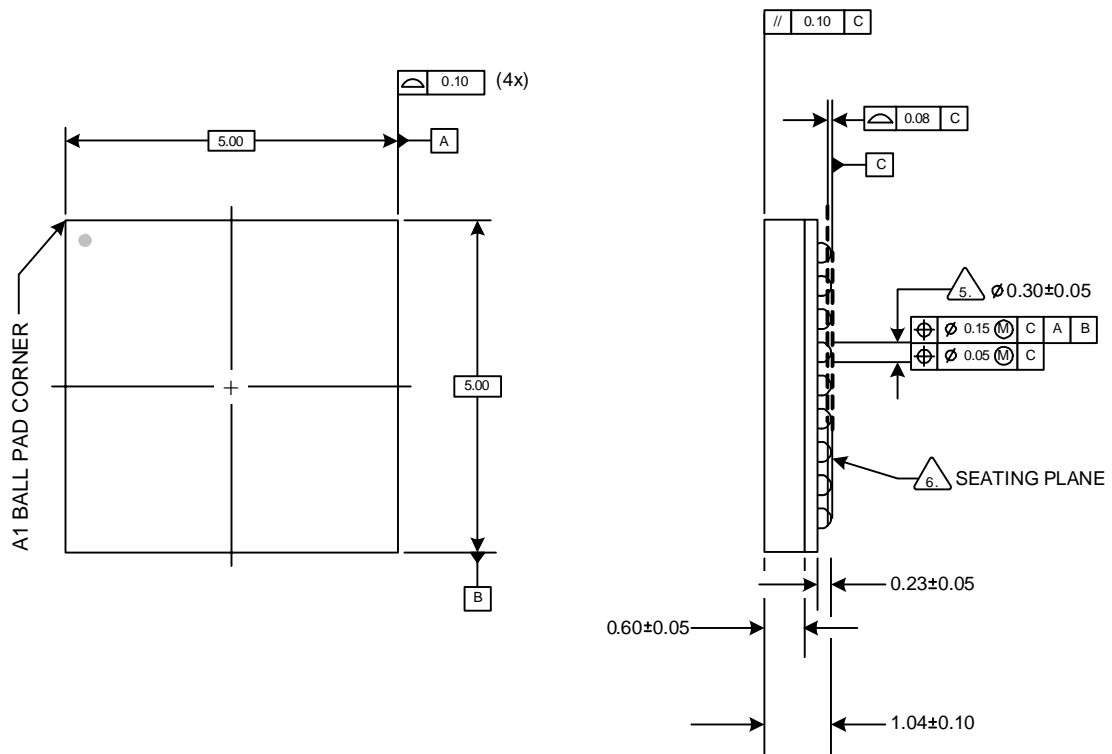


Figure 4-3 Chip Top and Side View